# EXHIBIT 1

**Silicon Valley Expert Witness Group, Inc.**
**An LECG Company**
**Consultant Curriculum Vitae**

# Richard A. Blanchard, Ph.D.

## Expertise

- MOS and Bipolar Device Technology
- Semiconductor Device Physics
- Microchip Fabrication & Analysis
- Electronic Systems
- Electrical & Electronic Failures
- CMOS, DMOS & BiCMOS
- Power IC's & Power Electronics
- Printed Circuit Board Manufacturing
- Semiconductor Process & Control
- Semiconductor Process Equipment

## Professional Summary

Dr. Blanchard has over 35 years of combined industry, research, academic, and consulting experience. His research covers semiconductor device and electronics design, semiconductor device physics, semiconductor manufacturing processes and equipment, failure analysis, reverse engineering of semiconductor and electronic circuits, and reliability modeling. Dr. Blanchard's work has resulted in more that 120 U.S. issued patents. He has also written or co-authored numerous books and articles in the semiconductor design and process development areas as well as failure analysis.

## Employment History

From: 1998 **Silicon Valley Expert Witness Group, Inc.**
To: Date Mountain View, CA
Position: *Director, Advanced Technologies*
Silicon Valley Expert Witness Group, Inc. (SVEWG) is a high technology, "Silicon Valley" consulting company specializing in expert witness litigation support and technology consulting. SVEWG has an extensive roster of world-class technology experts used in the defense and promotion of intellectual property rights and other litigation disputes. SVEWG Principals offer extensive in-house technology, legal and business expertise and have direct access to senior litigation and technology consultants worldwide.

From: 1991 **Failure Analysis Associates, Inc. (Now named "Exponent")**
To: 1998 Menlo Park, CA
Position: *Principal Engineer & Division Manager*
Responsible for the Electrical/Electronic Division of Failure Analysis Associates providing consulting services to the electrical

and electronics industry. Specific duties include:

- Semiconductor devices. Failure analysis and reverse engineering of solid-state electronic components and circuits. Semiconductor processing and semiconductor process equipment. Semiconductor manufacturing and process control.
- Failure analysis of electric and electronic systems, subsystems, and components, including causes of electrical fires
- Reliability modeling and lifetime prediction of electrical and electronic systems and subsystems
- Automotive electronics. Design of discrete devices and integrated circuits
- Power Electronics. Power MOS and Smart Power Technologies

From: 1987 **IXYS Corporation**
To: 1991
Position: *Senior Vice President*
Responsible for the development of IC products. Established an in-house CAD capability. Recruited an IC design team and coordinated the definition and development of IXYS ICs. Identified, qualified and monitored the IC foundries that manufactured these circuits. Set up testing capability at IXYS. Coordinated assembly on IC's. Worked on various MOSFET and IGBT device, test, and assembly problems.

From: 1982 **Siliconix, Inc.**
To: 1987
Position: *Vice President, Engineering*
Other titles held at Siliconix, Inc. were Engineering Manager (1982-1983) and Director (1983-1984). Responsible for the development of advanced process technology and the design of both discrete devices (JFETs, lateral and vertical DMOS transistors) and integrated circuits (low and high voltage CMOS, D/CMOS and bipolar-JFET). These responsibilities included providing technical and administrative direction to two IC design groups in the United Kingdom and the U.S., one device and process design group and a "quick-turn" processing line. Two CAD groups, one in the U.K. and one in the U.S., and a CAE group developing computer software and hardware for the engineering community rounded out the department. Personally responsible for many key innovations and inventions in power MOS and D/CMOS IC technology and their assembly and test requirements. He submitted approximately 20 patent disclosures while employed at Siliconix, Inc. He holds the two key "trench FET" patents, of which he is the sole inventor.

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From: 1976 **Supertex, Inc.**
To: 1982
Position: *Founder and Vice President, MOS Power Products*
Responsible for investigation of new semiconductor devices and new technologies. In charge of Power MOS device research, design and development. His work lead to the design and development of both the discrete power MOS device family and the high voltage IC (HVIC) family sold by Supertex, Inc. Responsible for an in-house assembly area as well as engineering aspects of power MOS and HVIC testing.

From: 1976 **Cognition, Inc.**
To: 1978
Position: *Founder and Consulting Engineer*
Responsible for developing the process technology for fabricating monolithic silicon pressure sensors. A process line was established for the manufacture of piezoresistive pressure sensors, including the precision etching of thin silicon diaphragms.

From: 1974 **Foothill College**
To: 1978
Position: *Associate Professor, Assistant Division Chairman, Engineering & Technology Division*
Accomplishments included developing the curriculum for the Semiconductor Technology Program, and establishing a small processing facility for teaching students the fundamentals of semiconductor technology. Supervised approximately 60 instructors in the evening and off-campus programs.

From: 1974 **Independent Consultant**
To: 1976
Duties: Consultant to the semiconductor industry, including court appointed "Special Master" in the Fairchild Semiconductor Corporation v. National Semiconductor Corporation Isoplanar patent suit.

From: 1970 **Fairchild Semiconductor**
To: 1974 Mountain View, CA
Position: *Senior Engineer, Department Manager*
Responsible for the fabrication of the integrated circuits in the Polaroid SX-70 camera. Technologies directly related to this work include standard bipolar technology, bipolar- MOS technology, silicon gate technology and flip-chip assembly technology.

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## Deposition and Trial Testimony (Past Five Years)

Apple Computer, Inc. v. Tatung Co., International Court of Arbitration of the International Chamber of Commerce, Case No. 10099 AER. (D, R)

Anne Camilleri as Guardian for Andrea Camilleri, an incompetent Adult, vs. Costco Companies, Inc., Thompson Merchandising, Everstar Merchandise, So Yang Enterprises Co. Ltd. And Does 1 to 1000. Superior Court of the State of California, County of San Mateo, Case No. 407 06 & Case No. 408 615. (D)

Micrel, Inc. v. Federal Insurance Company, Superior Court of the State of California and Santa Clara County, Case No. CV786627. (D, R)

Sun Microsystems v. Kingston Technology, United States District Court, Northern District of California, Case No. C99-03610VRW. (D, R)

Level One v. Altima, United States International Trade Commission, Washington, D.C., Investigation No. 337-TA-435. (D, R, T)

Optus Networks Pty Ltd CAN 008 570 330 and Ors v. Leighton Contractors Pty Ltd CAN 000 893 667 and Ors, Supreme Court of New South Wales Sydney Registry Common Law Division Construction List, No. 55059 of 1997. (R, T)

Federal Insurance Company v. Metex Corporation, Superior Court of the State of California, County of San Francisco, No. 988899. (D, R)

Pekin Insurance Company and Green Bay Motor Sports, Inc. v. American Suzuki Motor Corporation, Circuit Court of the State of Wisconsin, County of Brown, No. 01-CV-416 (4/2002). (D)

Kenneth Toner and Daniel J. Harper, as Trustee of the Recall Claimants Trust v. Cadet Manufacturing Company, I.R.C.A. S.P.A., Zoppas Industries S.P.A. and Still-man Heating Products Inc., Superior Court of the State of Washington, County of King, No. 98-2-10876-2SEA (4/2002). (D)

Allen Scott Schneider, Tami Schneider v. Sentry Alarm, Inc., Sylvester's Alarm, Inc. a.k.a. Sylvester's Security Services, Inc. Automatic Alarm, Inc., Superior Court of the State of California, County of Santa Clara, Case No. CV 795867. (D)

David Bryte, Personal Representative of the Estate of Lova E. Bryte, deceased, et al, plaintiffs v. Sunbeam Corporation & Sears Roebuck and Co., defendants. In the United States District Court for the Northern District of West Virginia, Case No. 2:00-CV-93. (D, R)

SimpleTech, Inc. v. Atmel Corporation, Superior Court of the State of California, County of Santa Clara, Case No. CV 809851 (2004). (D, R)

Pavel Kuzmenko; Karina Kuzmenko and Kristina Kuzmenko v. Morningside Apartments, William R. Canihan, and MacFrugal's Bargain Close Out, Superior Court of the State of California, County of Sacramento, Case No. 01AS00112 (2004). (D)

State Farm Fire & Casualty Insurance Company; as subrogee for Terry Swan, and Terry Swan, individually v. Sears, Roebuck and Co., a foreign corporation, the United States District Court for the Western District of Washington, Case No. C01-129 (C). (D, R)

Rexford Agin, Susan Agin and Daniel Agin v. Sunbeam Products, Inc., in the United States District Court for the Southern District of Ohio Eastern Division, Civil Action No. C2030052. (D, R)

Bobby Cook, as Personal Representative of the Estate of Cathy Lynn Cook, Deceased; and Bobby Cook, Individually v. Sunbeam Corporation, Sunbeam Products, Inc., Wal-Mart Stores, Inc., and Wal-Mart Stores, East, Inc., United States District Court for the Northern District of Alabama Southern Division, Case No. CV-01-B-2000-S. (D, R)

IXYS Corporation v. Advanced Power Technology, Inc., United States District Court for the Northern District of California San Francisco Division, Case No. C 02-3942 MHP. (D, R)

Motorola, Inc. v. Analog Devices, Inc., United States District Court for the Eastern District of Texas Beaumont Division, Civil Action No. 1:03-CV-0131 (RHC). (D, R)

Siliconix Inc., a Delaware corporation v. Alpha and Omega Semiconductor Inc., a California corporation, and Alpha and Omega Semiconductor Limited, a Bermuda corporation, United States District Court for the Northern District of California San Francisco Division, Case No. C03-04803 WHA (Inventor). (D)

Sunex, Inc. v. Omnivision Technologies/Omnivision Technologies, Inc., a Delaware Corporation v. Sunex, Inc, Superior Court of the State of California County of San Diego, North County Division, Case No. 031205. (D)

Fujitsu Limited v. Cirrus Logic, Inc., Amkor Technology, Inc., Sumitomo Bakelite Co., Ltd., and Sumitomo Plastics America, Inc., Superior Court of the State of California County of Santa Clara, Case. No. 1-03-CV-009885. (D)

Silicon Laboratories, Inc. v. Ali Niknejad & Axiom Microdevices, Inc., United States District Court for the Western Division of Texas Austin Division, Civil Action No. A-04-CA-155-SS. (D, T)

Joel R. Bertelson, Daniel E. Mendl, Daniel E. Mendl as Trustee, The Bigfoot Ranch, II, Inc., Daniel E. Mendl as Attorney In Fact for Katherine Hope Bertelson and Union Mutual Fire Insurance Co. and New England Guaranty Insurance Co., Inc. v. Sunbeam Products, Inc. and The Allen Agency, Inc., Superior Court of the State of Vermont Chittenden County, SS, Docket No. S0312-04 CnC. (D)

Micrel Inc. v. Monolithic Power Systems, Michael R. Hsing, James C. Moyer, and DOES 1-20 inclusive, Unites States District Court for the Northern District of California San Francisco Division, Case No. C04-04770 JSW (JCS). (D)

Siliconix, Inc. v. Denso Corporation, United States District Court for the Northern District of California, San Francisco Division, Case No. C05-01507 WHA and Consolidated Actions Nos. C04-00344 WHA and C05-03617 WHA. (D)

Tessera, Inc. v. Micron Technology, Inc. and Infineon, United States District Court for the Eastern District of Texas Marshall Division, Case No. 2-05CV94. (R)

Siliconix, Inc. v. Semiconductor Components Industries, LLC d/b/a On Semiconductor, American Arbitration Association, Phoenix, Arizona, Case No. 76 133 Y 00327 05 DEAR. (D)

John Rumans, Jeanne Rumans and Jessica Rumans v. Sunbeam Products, Inc., United States District Court for the Western District of Missouri Western Division, Case No. 05-1226-CV-W-HFS. (D)

Markel American Insurance Company, Insurance Company of North America and State Farm Fire and Casualty Company v. Cadet Heater Manufacturing Company v. ZIMM (Third-Party Defendants), United States District Court for the District of Oregon, Case No. 3:05-CV-1188 KI (Lead Case). (D, R)

Verigy US, Inc. v. Romi Omar Mayder, Wesley Mayder, Silicon Test Systems, Inc., and Silicon Test Solutions, LLC, United States District Court for the Northern District of California San Jose Division, Case No. C07-04330 RMW (HRL). (D)

Nathan J. Sheridan v. Fladeboe Volkswagen, Inc., Volkswagen of America, Inc., Superior Court of the State of California for the County of Orange, Case No. 06CC09510. (D)

Quantum Research Group v. Apple Computer Company, Inc., Cypress Semiconductor Corp., Cypress Microsystems, and Fingerworks, Inc., Unites States District of Maryland, Civil Action No. 1:05-CV-03408-WMN. (D)

D = Deposition
R = Report
T = Testimony in Court

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## Patents

| Patent Number | Date Issued | Title |
|---|---|---|
| 7,244,970 | 07/17/2007 | Low Capacitance Two-Terminal Barrier Controlled TVS Diodes |
| 7,224,027 | 05/29/2007 | High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching and Diffusion from Regions of Oppositely Doped Polysilicon |
| 7,202,494 | 04/10/2007 | FinFET Including a Supperlattice |
| 7,199,427 | 04/03/2007 | DMOS Device with a Programmable Threshold Voltage |
| 7,138,289 | 11/21/2006 | Technique for Fabricating Multilayer Color Sensing Photodetectors |
| 7,094,621 | 08/22/2006 | Fabrication on diaphragms and 'Floating' Regions of Single Crystal Semiconductor for MEMS Devices |
| 7,091,552 | 08/15/2006 | High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching and Ion Implantation |
| 7,084,455 | 08/01/2006 | Power Semiconductor Device Having a Voltage Sustaining Region that Includes Terraced Trench with Continuous Doped Columns Formed in an Epitaxial Layer |
| 7,067,376 | 06/27/2006 | High Voltage power MOSFET Having Low On-Resistance |
| 7,061,072 | 06/13/2006 | Integrated Circuit Inductors Using Driven Shields |
| 7,023,069 | 04/04/2006 | Method for Forming Thick Dielectric Regions Using Etched Trenches |
| 7,019,360 | 03/28/2006 | High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching Using an Etchant Gas that is also a Doping Source |
| 7,015,104 | 03/21/2006 | Technique for Forming the Deep Doped Columns in Superjunction |
| 6,992,350 | 01/31/2006 | High Voltage Power MOSFET Having Low On-Resistance |
| 6,949,432 | 09/27/2005 | Trench DMOS Transistor Structure Having a Low Resistance Path to a Drain Contact Located on an Upper Surface |
| 6,921,938 | 07/26/2005 | Double Diffused Field Effect Transistor Having Reduced On-Resistance |
| 6,906,529 | 06/14/2005 | Capacitive Sensor Device With Electrically Configurable Pixels |
| 6,882,573 | 04/19/2005 | DMOS Device with a Programmable Threshold Voltage |
| 6,861,337 | 03/01/2005 | Method for Using a Surface Geometry for a MOS-Gated Device in the Manufacture of Dice Having Different Sizes |
| 6,812,526 | 11/02/2004 | Trench DMOS Transistor Structure Having a Low Resistance Path to a Drain Contact Located on an Upper Surface |
| 6,812,056 | 11/02/2004 | Technique for Fabricating MEMS Devices Having Diaphragms of "Floating" Regions of Single Crystal Material |
| 6,794,251 | 09/21/2004 | Method of Making a Power Semiconductor Device |
| 6,790,745 | 09/14/2004 | Fabrication of Dielectrically Isolated Regions of Silicon in a Substrate |
| 6,777,745 | 08/17/2004 | Symmetric Trench MOSFET Device and Method of Making Same |
| 6,750,523 | 06/15/2004 | Photodiode Stacks for Photovoltaic Relays and the Method of Manufacturing the Same |

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| 6,750,104 | 06/15/2004 | High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching Using an Etchant Gas that is also a Doping Source |
| 6,734,495 | 05/11/2004 | Two Terminal Programmable MOS-Gated Current Source |
| 6,730,963 | 05/04/2004 | Minimum Sized Cellular MOS-Gated Device Geometry |
| 6,724,044 | 04/20/2004 | MOSFET Device Having Geometry that Permits Frequent Body Contact |
| 6,724,039 | 04/20/2004 | Semiconductor Device Having a Schottky Diode |
| 6,713,351 | 03/30/2004 | Double Diffused Field Effect Transistor Having Reduced On-Resistance |
| 6,710,414 | 03/23/2004 | Surface Geometry for a MOS-Gated Device that Allows the Manufacture of Dice Having Different Sizes |
| 6,710,400 | 03/23/2004 | Method for Fabricating a High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Rapid Diffusion |
| 6,689,662 | 02/10/2004 | Method of Forming a Higher Voltage Power MOSFET Having Low On-Resistance |
| 6,686,244 | 02/03/2004 | Power Semiconductor Device Having a Voltage Sustaining Region that Includes Doped Columns Formed with a Single Ion Implantation Step |
| 6,660,571 | 12/09/2003 | High Voltage Power MOSFET Having Low On-Resistance |
| 6,656,797 | 12/02/2003 | High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching and Ion Implantation |
| 6,649,477 | 11/18/2003 | Method for Fabricating a Power Semiconductor Device Having a Voltage Sustaining Layer with a Terraced Trench Facilitating Formation of Floating Islands |
| 6,627,949 | 09/30/2003 | High Voltage Power MOSFET Having Low On-Resistance |
| 6,624,494 | 09/23/2003 | Method for Fabricating a Power Semiconductor Device Having a Floating Island Voltage Sustaining Layer |
| 6,621,107 | 09/16/2003 | Trench DMOS Transistor with Embedded Trench Schottky Rectifier |
| 6,593,619 | 07/15/2003 | High Voltage Power MOSFET Having Low On-Resistance |
| 6,593,174 | 07/15/2003 | Field Effect Transistor Having Dielectrically Isolated Sources and Drains and Method for Making Same |
| 6,576,516 | 06/10/2003 | High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Trench Etching and Diffusion from Regions of Oppositely Doped Polysilicon |
| 6,566,201 | 05/20/2003 | Method for Fabricating a High Voltage Power MOSFET Having a Voltage Sustaining Region that Includes Doped Columns Formed by Rapid Diffusion |
| 6,538,279 | 03/25/2003 | High-Side Switch With Depletion-Mode Device |
| 6,492,663 | 12/10/2002 | Universal Source Geometry for MOS-Gated Power Devices |
| 6,479,352 | 11/12/2002 | Method of Fabricating High Voltage Power MOSFET Having Low On-Resistance |

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| 6,472,709 | 10/29/2002 | Trench DMOS Transistor Structure Having a Low Resistance Path to a Drain Contact Located on an Upper Surface |
| 6,468,866 | 10/22/2002 | Single Feature Size MOS Technology Power Device |
| 6,465,304 | 10/15/2002 | Method for Fabricating a Power Semiconductor Device Having a Floating Island Voltage Sustaining Layer |
| 6,432,775 | 08/13/2002 | Trench DMOS Transistor Structure Having a Low Resistance Path to a Drain Contact Located on an Upper Surface |
| 6,420,764 | 07/16/2002 | Field Effect Transistor Having Dielectrically Isolated Sources and Drains and Methods for Making Same |
| 6,403,427 | 06/11/2002 | Field Effect Transistor Having Dielectrically Isolated Sources and Drains and Method for Making Same |
| 6,399,961 | 06/04/2002 | Field Effect Transistor Having Dielectrically Isolated Sources and Drains and Method for Making Same |
| 6,369,426 | 04/09/2002 | Transistor with Integrated Photodetector for Conductivity Modulation |
| 6,368,918 | 04/09/2002 | Method of Fabricating an Embedded Flash EEPROM with a Tunnel Oxide Grown on a Textured Substrate |
| 6,331,794 | 12/18/2001 | Phase Leg with Depletion-mode Device |
| 6,316,336 | 11/13/2001 | Method for Forming Buried Layers With Top-Side Contacts and the Resulting Structure |
| 6,291,845 | 19/18/2001 | Fully-Dielectric-Isolated FET Technology |
| 6,272,050 | 08/07/2001 | Method and Apparatus for Providing an Embedded Flash-EEPROM Technology |
| 6,239,752 | 05/29/2001 | Semiconductor Chip Package that is also an Antenna |
| 6,225,662 | 05/01/2001 | Semiconductor Structure with Heavily Doped Buried Breakdown Region |
| 6,215,170 | 04/10/2001 | Structure for Single Conductor Acting as Ground and Capacitor Plate Electrode Using Reduced Area |
| 6,198,114 | 03/06/2001 | Field Effect Transistor Having Dielectrically Isolated Sources and Drains and Method for Making Same |
| 6,069,385 | 05/30/2000 | Trench MOS-Gated Device |
| 6,064,109 | 05/16/2000 | Ballast Resistance for Producing Varied Emitter Current Flow Along the Emitter's Injecting Edge |
| 6,046,473 | 04/04/2000 | Structure and Process for Reducing the On-Resistance of MOS-Gated Power Devices |
| 6,011,298 | 01/04/2000 | High Voltage Termination with Buried Field-Shaping Region |
| 5,985,721 | 11/16/1999 | Single Feature Size MOS Technology Power Device |
| 5,981,998 | 11/09/1999 | Single Feature Size MOS Technology Power Device |
| 5,981,318 | 11/09/1999 | Fully-dielectric-isolated FET Technology |
| 5,960,277 | 09/28/1999 | Method of Making a Merged Device with Aligned Trench FET and Buried Emitter Patterns |
| 5,897,355 | 05/27/1999 | Method of Manufacturing Insulated Gate Semiconductor Device to Improve Ruggedness |
| 5,869,371 | 02/09/1999 | Structure and Process for Reducing the On-Resistance of MOS-gated |

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|---|---|---|
| | | Power Devices |
| 5,856,696 | 01/05/1999 | Field Effect Transistor Having Dielectrically Isolated Sources and Drains |
| 5,821,136 | 10/13/1998 | Inverted Field-Effect Device with Polycrystalline Silicon/Germanium Channel |
| 5,801,396 | 09/01/1998 | Inverted Field-Effect Device with Polycrystalline Silicon/Germanium Channel |
| 5,798,549 | 08/25/1998 | Conductive Layer Overlaid Self-Aligned MOS-Gated Semiconductor Devices |
| 5,773,328 | 06/30/1998 | Method Of Making A Fully-Dielectric-Isolated Fet |
| 5,756,386 | 05/26/1998 | Method of Making Trench MOS-Gated Device with A Minimum Number of Masks |
| 5,710,443 | 01/20/1998 | Merged Device with Aligned Trench Fet and Buried Emitter Patterns |
| 5,708,289 | 01/13/1998 | Pad Protection Diode Structure |
| 5,701,023 | 12/23/1997 | Insulated Gate Semiconductor Device Typically Having Subsurface-Peaked Portion of Body Region For Improved Ruggedness |
| 5,691,555 | 11/25/1997 | Integrated Structure Current Sensing Resistor For Power Devices Particularly For Overload Self-Protected Power MOS Devices |
| 5,668,025 | 09/16/1997 | Method of Making a FET with Dielectrically Isolated Sources and Drains |
| 5,663,079 | 09/02/1997 | Method of Making Increased Density MOS-Gated Semiconductor Devices |
| 5,648,670 | 07/15/1997 | Trench MOS-Gated Device with a Minimum Number of Masks |
| 5,640,037 | 06/17/1997 | Cell with Self-Aligned Contacts |
| 5,637,889 | 06/10/1997 | Composite Power Transistor Structures Using Semiconductor Materials With Different Bandgaps |
| 5,589,415 | 12/31/1996 | Method For Forming a Semiconductor Structure with Self-Aligned Contacts |
| 5,576,245 | 11/19/1996 | Method of Making Vertical Current Flow Field Effect Transistor |
| 5,574,301 | 11/12/1996 | Vertical Switched-Emitter Structure with Improved Lateral Isolation |
| 5,528,063 | 06/18/1996 | Conductive-Overlaid Self-Aligned MOS-Gated Semiconductor Devices |
| 5,485,027 | 01/16/1996 | Isolated DMOS IC Technology |
| 5,298,781 | 03/29/1994 | Vertical Current Flow Field Effect Transistor with Thick Insulator Over Non-Channel Areas |
| 5,237,481 | 08/17/1993 | Temperature Sensing Device for Use in a Power Transistor |
| 5,218,228 | 06/08/1993 | High Voltage MOS Transistors with Reduced Parasitic Current Gain |
| 5,164,325 | 11/17/1992 | Method of Making a Vertical Current Flow Field Effect Transistor |
| 5,156,989 | 10/20/1992 | Complementary Isolated DMOS IC Technology |
| 5,132,235 | 07/21/1992 | Method for Fabricating a High Voltage MOS Transistor |
| 5,034,785 | 07/23/1992 | Planar Vertical Channel DMOS Structure |
| 4,983,535 | 01/08/1991 | Vertical DMOS Transistor Fabrication Process |
| 4,978,631 | 12/18/1990 | Current Source with a Process Selectable Temperature Coefficient |

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| 4,958,204 | 09/18/1990 | Junction Field-Effect Transistor with a Novel Gate |
| 4,956,700 | 19/11/1990 | Integrated Circuit with High Power, Vertical Output Transistor Capability |
| 4,952,992 | 08/28/1990 | Method and Apparatus for Improving the On-Voltage Characteristics of a Semiconductor Device |
| 4,929,991 | 05/29/1990 | Rugged Lateral DMOS Transistor Structure |
| 4,920,388 | 04/24/1990 | Power Transistor with Integrated Gate Resistor |
| 4,916,509 | 04/10/1990 | Method for Obtaining Low Interconnect Resistance on a Grooved Surface and the Resulting Structure |
| 4,914,058 | 04/03/1990 | Grooved DMOS Process with Varying Gate Dielectric Thickness |
| 4,896,196 | 01/23/1990 | Vertical DMOS Power Transistor with an Integral Operating Condition Sensor |
| 4,893,160 | 01/09/1990 | Method for Increasing the Performance of Trenched Devices and the Resulting Structure |
| 4,868,537 | 09/19/1989 | Doped $Si0_2$ Resistor and Method of Forming Same |
| 4,851,366 | 07/25/1989 | Method for Providing Dielectrically Isolated Circuit |
| 4,845,051 | 07/04/1989 | Buried Gate JFET |
| 4,832,586 | 05/30/1989 | Dual-Gate High Density FET |
| 4,827,324 | 05/02/1989 | Implantation of Ions into an Insulating Layer of Increase Planar PN Junction Breakdown Voltage |
| 4,824,795 | 04/25/1989 | Method for Obtaining Regions of Dielectrically Isolated Single Crystal Silicon |
| 4,813,882 | 03/28/1989 | Power MOS Transistor with Equipotential Ring |
| 4,799,100 | 01/17/1989 | Method and Apparatus for Increasing Breakdown of a Planar Junction |
| 4,798,810 | 01/17/1989 | Method for Manufacturing a Power MOS Transistor |
| 4,794,436 | 12/27/1988 | High Voltage Drifted-Drain MOS Transistor |
| 4,791,462 | 12/13/1988 | Dense Vertical J-MOS Transistor |
| 4,774,196 | 09/27/1988 | Method of Bonding Semiconductor Wafers |
| 4,767,722 | 08/30/1988 | Method for Making Planar Vertical Channel DMOS Structures |
| 4,759,836 | 07/26/1988 | Ion Implantation of Thin Film $CrSi_2$ and SiC Resistors |
| 4,707,909 | 11/24/1987 | Manufacture of Trimmable High Value Polycrystalline Silicon Resistors |
| 4,682,405 | 07/28/1987 | Method for Forming Lateral and Vertical DMOS Transistors |
| 4,402,003 | 08/30/1983 | Composite MOS/Bipolar Power Device |
| 4,398,339 | 08/16/1983 | Fabrication Method for High Power MOS Device |
| 4,393,391 | 07/12/1988 | Power MOS Transistor With a Plurality of Longitudinal Grooves to Increase Channel Conducting Area |
| 4,345,265 | 08/17/1982 | MOS Power Transistor with Improved High-Voltage Capability |
| 4,344,081 | 08/10/1982 | Combined DMOS and a Vertical Device and Fabrication Method Therefore |
| 4,145,703 | 03/20/1979 | High Power MOS Device and Fabrication Method Therefore |

**Silicon Valley Expert Witness Group, Inc.**
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## Education

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|---|---|---|
| 1982 | Stanford University | Ph.D., Electrical Engineering<br>Thesis: "Optimization of Discrete High Power MOS Transistors." |
| 1970 | M.I.T. | MSEE<br>Thesis: "The Use of a Thermal Feedback Mechanism in Power Transistor Structures." |
| 1968 | M.I.T. | BSEE |

## Publications – Books

Blanchard, R. A., Burgess, David, "Wafer Failure Analysis for Yield Enhancement," *Accelerated Analysis,* 2000.

Blanchard, R.A., "Electronic Failure Analysis Handbook," co-author of three chapters, P. L. Martin, ed., *McGraw-Hill,* 1999.

Blanchard, R.A., Trapp, O., Lopp, L., "Semiconductor Technology Handbook," Portola Valley, California, *Technology Associates*, 1993.

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## Professional Associations and Achievements

- Senior Member, Institute of Electrical and Electronics Engineers
- Member, Electronic Device Failure Analysis Society
- Member, International Microelectronics & Packaging Society
- Member, American Vacuum Society
- Member, National Fire Protection Association
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# EXHIBIT 2

**EXHIBIT A**

ACKNOWLEDGMENT AND AGREEMENT TO BE BOUND

I, Richard A. Blanchard [print or type full name], of 10724 Moca Dr., Los Altos, CA 94024 [print or type full address], declare under penalty of perjury that I have read in its entirety and understand the Stipulated Protective Order (the "Order") that was issued by the United States District Court for the Northern District of California on August 1, 2007 [date] in the case of C 07-02664 JSW (the "Action"). I agree to comply with and to be bound by all the terms of this Order and I understand and acknowledge that failure to so comply could expose me to sanctions and punishment in the nature of contempt. I solemnly promise that I will not disclose in any manner any information or item that is subject to this Order to any person or entity except in strict compliance with the provisions of this Order.

I further agree to submit to the jurisdiction of the United States District Court for the Northern District of California for the purpose of enforcing the terms of this Order, even if such enforcement proceedings occur after termination of this Action.

Date: August 10, 2007

City and State where sworn and signed: Mt. View, CA

Printed name: Richard A. Blanchard
[printed name]

Signature: Richard A. Blanchard
[signature]

# EXHIBIT 3

US006429481B1

(12) **United States Patent**
**Mo et al.**

(10) **Patent No.: US 6,429,481 B1**
(45) **Date of Patent: *Aug. 6, 2002**

(54) **FIELD EFFECT TRANSISTOR AND METHOD OF ITS MANUFACTURE**

(75) Inventors: **Brian Sze-Ki Mo**, Fremont; **Duc Chau**, San Jose; **Steven Sapp**, Felton; **Izak Bencuya**, Saratoga, all of CA (US); **Dean Edward Probst**, West Jordan, UT (US)

(73) Assignee: **Fairchild Semiconductor Corporation**, South Portland, MA (US)

( * ) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **08/970,221**

(22) Filed: **Nov. 14, 1997**

(51) **Int. Cl.**[7] ..... **H01L 29/78**
(52) **U.S. Cl.** ..... **257/341**; 257/331
(58) **Field of Search** ..... 257/330, 245, 257/497, 618, 341, 331

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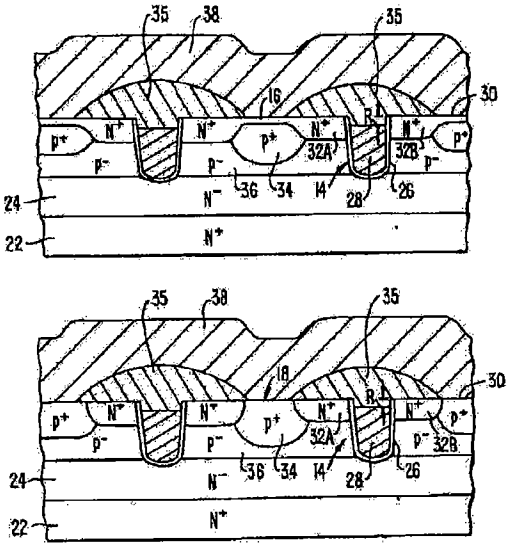
*Primary Examiner*—Jerome Jackson, Jr.
(74) *Attorney, Agent, or Firm*—Townsend and Townsend and Crew LLP

(57) **ABSTRACT**

A trenched field effect transistor is provided that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

**22 Claims, 9 Drawing Sheets**





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US006710406B2

(12) **United States Patent**
**Mo et al.**

(10) **Patent No.: US 6,710,406 B2**
(45) **Date of Patent: *Mar. 23, 2004**

(54) **FIELD EFFECT TRANSISTOR AND METHOD OF ITS MANUFACTURE**

(75) Inventors: **Brian Sze-Ki Mo**, Fremont, CA (US); **Duc Chau**, San Jose, CA (US); **Steven Sapp**, Felton, CA (US); **Izak Bencuya**, Saratoga, CA (US); **Dean Edward Probst**, West Jordan, UT (US)

(73) Assignee: **Fairchild Semiconductor Corporation**, South Portland, ME (US)

( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 35 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **10/155,554**

(22) Filed: **May 24, 2002**

(65) **Prior Publication Data**

US 2002/0140027 A1 Oct. 3, 2002

**Related U.S. Application Data**

(63) Continuation of application No. 08/970,221, filed on Nov. 14, 1997, now Pat. No. 6,429,481.

(51) **Int. Cl.**[7] ..... **H01L 29/78**
(52) **U.S. Cl.** ..... **257/341**; 257/331
(58) **Field of Search** ..... 257/331, 341

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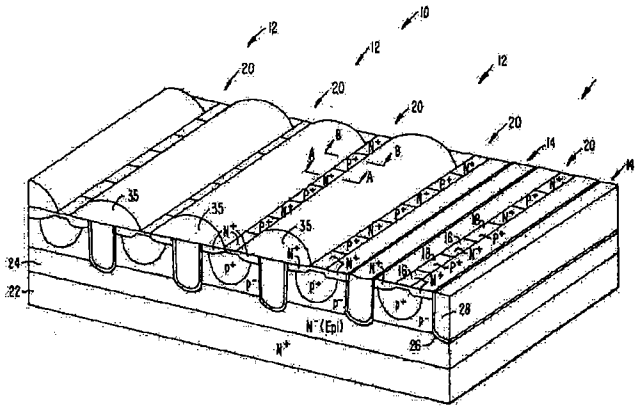
*Primary Examiner*—Jerome Jackson
(74) *Attorney, Agent, or Firm*—Babak S. Sani; Townsend and Townsend and Crew LLP

(57) **ABSTRACT**

A trenched field effect transistor is provided that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

**32 Claims, 9 Drawing Sheets**





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US006828195B2

(12) **United States Patent**
**Mo et al.**

(10) **Patent No.: US 6,828,195 B2**
(45) **Date of Patent: Dec. 7, 2004**

(54) **METHOD OF MANUFACTURING A TRENCH TRANSISTOR HAVING A HEAVY BODY REGION**

(75) Inventors: **Brian Sze-Ki Mo**, Fremont, CA (US); **Duc Chau**, San Jose, CA (US); **Steven Sapp**, Felton, CA (US); **Izak Bencuya**, Saratoga, CA (US); **Dean Edward Probst**, West Jordan, UT (US)

(73) Assignee: **Fairchild Semiconductor Corporation**, South Portland, ME (US)

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(21) Appl. No.: **10/347,254**

(22) Filed: **Jan. 17, 2003**

(65) **Prior Publication Data**

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**Related U.S. Application Data**

(60) Continuation of application No. 09/854,102, filed on May 9, 2001, now Pat. No. 6,521,497, which is a division of application No. 08/970,221, filed on Nov. 14, 1997, now Pat. No. 6,429,481.

(51) **Int. Cl.**[7] ..... **H01L 21/336**

(52) **U.S. Cl.** ..... **438/270**; 438/589

(58) **Field of Search** ..... 438/270–272, 438/589

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*Primary Examiner*—John F. Niebling
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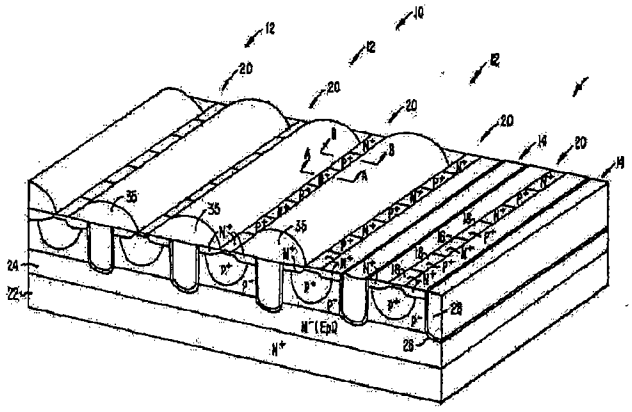
(74) *Attorney, Agent, or Firm*—Babak S. Sani; Townsend and Townsend and Crew LLP

(57) **ABSTRACT**

A trenched field effect transistor is provided that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

**23 Claims, 9 Drawing Sheets**

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US007148111B2

(12) **United States Patent**
**Mo et al.**

(10) **Patent No.: US 7,148,111 B2**
(45) **Date of Patent: *Dec. 12, 2006**

(54) **METHOD OF MANUFACTURING A TRENCH TRANSISTOR HAVING A HEAVY BODY REGION**

(75) Inventors: **Brian Sze-Ki Mo**, Fremont, CA (US); **Duc Chau**, San Jose, CA (US); **Steven Sapp**, Felton, CA (US); **Izak Bencuya**, Saratoga, CA (US); **Dean E. Probst**, West Jordan, UT (US)

(73) Assignee: **Fairchild Semiconductor Corporation**, San Jose, CA (US)

( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **10/927,788**

(22) Filed: **Aug. 27, 2004**

(65) **Prior Publication Data**

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**Related U.S. Application Data**

(60) Continuation of application No. 10/347,254, filed on Jan. 17, 2003, now Pat. No. 6,828,195, which is a continuation of application No. 09/854,102, filed on May 9, 2001, now Pat. No. 6,521,497, which is a division of application No. 08/970,221, filed on Nov. 14, 1997, now Pat. No. 6,429,481.

(51) **Int. Cl.**
***H01L 21/336*** (2006.01)

(52) **U.S. Cl.** ..... **438/270**; 438/272; 438/589

(58) **Field of Classification Search** ..... 438/270, 438/272, 589

See application file for complete search history.

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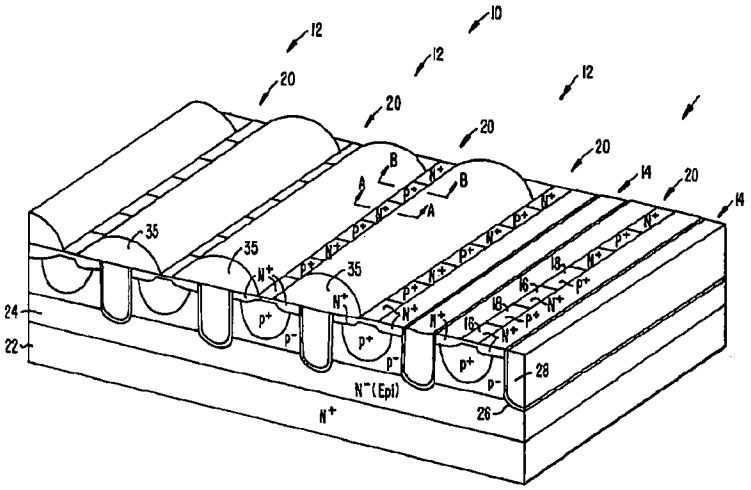
*Primary Examiner*—Lynne A. Gurley
(74) *Attorney, Agent, or Firm*—Babak S. Sani; Townsend and Townsend and Crew LLP

(57) **ABSTRACT**

A trenched field effect transistor is provided that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

**36 Claims, 9 Drawing Sheets**





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# United States Patent [19]

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[54] **METHOD FOR DEVICE RUGGEDNESS IMPROVEMENT AND ON-RESISTANCE REDUCTION FOR POWER MOSFET ACHIEVED BY NOVEL SOURCE CONTACT STRUCTURE**

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[21] Appl. No.: **08/899,186**

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[52] **U.S. Cl.** ..... **438/268**; 438/307

[58] **Field of Search** ..... 438/138, 156, 438/268, 273, 307, 529, 545

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[57] **ABSTRACT**

The invention discloses method for fabricating a MOSFET on a substrate to improve device ruggedness. The method includes steps of: (a) forming an epi-layer of a first conductivity type as a drain region on the substrate and growing an initial oxide layer over the epi-layer; (b) applying an active mask for etching the active layer to define an active area followed by depositing an overlaying polysilicon layer and applying a polysilicon mask for etching the polysilicon layer to define a plurality of polysilicon gates; (c) removing the mask and carrying out a body implant of a second conductivity type followed by performing a body diffusion for forming a plurality of body regions; (d) applying a source blocking mask for implanting a plurality of source regions in the body regions with ions of the first conductivity type followed by removing the blocking mask and a source diffusion process; (e) forming an overlying insulation layer covering the MOSFET followed by applying a contact mask to open a plurality of contact openings; (f) performing a low energy body-dopant and high energy body dopant implant to form a shallow high-concentration body dopant and a deep high-concentration body dopant region followed by applying a high temperature process for densification of the insulation layer and activating diffusion of the deep and shallow body dopant regions wherein the deep high-concentration body-dopant regions are formed below the source regions and extends beyond the contact regions but are kept at lateral distance away from a channel region of the MOSFET in the body region whereby device ruggedness is improved without increasing threshold voltage.

**7 Claims, 13 Drawing Sheets**